UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,278	12/15/2004	Carl Christensen	PU020290	6691

7590 10/15/2008

Joseph S Tripoli
Thomson Licensing Inc
P O Box 5312
Princeton, NJ 08543-5312

EXAMINER	
RUTKOWSKI, JEFFREY M	
ART UNIT	PAPER NUMBER
2419	

MAIL DATE	DELIVERY MODE
10/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,278	CHRISTENSEN, CARL	
	Examiner	Art Unit	
	JEFFREY M. RUTKOWSKI	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-2 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuholm (US Pat 6,104,997) in view of Cooper et al. (US Pat 5,550,594), hereinafter referred to as Cooper and Watanabe et al. (US Pg Pub 2002/0031148), hereinafter referred to as Watanabe.

4. For **claims 1 and 2**, Shuholm teaches a digital audio receiver with multi-channel swapping **[title]**, used in a broadcast router **[col. 1 lines 25-35]**. The receiver has a first input for the first two channels of an Audio Engineering Society (AES) signal **12** (claim 1: first reference input) and a second input for the third and fourth channels of an AES signal **13** (claim 1: second reference input). A pair of selector circuits **20, 22** (claim 1: a reference select circuit) is used to assign data from the channel buffers to an output stream or to the position in an output stream **[col. 2 lines 40-43 and figure 4]**. The output streams are sent to a conventional matrix router

[col. 2 line 56] (claim 1: at least one router component coupled to said reference select circuit; claim 2: wherein said at least one router component further comprises a router matrix).

5. Shuholm does not teach a selection circuit that passes one signal in lieu of another error-free signal. Cooper teaches a selection circuit that passes an input signal as a reference signal when the reference signal has encountered an error, namely the reference signal is missing **[col. 16 lines 25-28]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Cooper's selection circuit in Shuholm's invention to provide an adjustable way to synchronize signals by allowing a clocking signal to come from more than one source **[Cooper, col. 4 lines 30-40]**.

6. The combination of Shuholm and Cooper disclose a selection mechanism that selects an error-free signal. The combination does not disclose a mechanism for selecting one reference signal over another reference signal. Watanabe teaches an integrated circuit that uses a two mode selector that selects either a second clocking signal or allows a first clocking signal to be applied redundantly **[0028, figure 1]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Watanabe's selection circuit in Shuholm's invention to allow for different sources to be used as a clocking signal **[Watanabe, 0008-0009]**.

7. For **claim 11**, the combination of Shuholm, Cooper and Watanabe disclose a hardware structure that operates on independent or redundant clock signals (reference signals) **[Watanabe, figure 1]**. Additionally, Watanabe's selector allows the router to operate without having to make modifications at the hardware level.

8. **Claims 3 and 4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuholm in view of Cooper and Watanabe as applied to **claim 1** above and further in view of Lydon et al. (US Pat. 6,680,939), hereinafter referred to as Lydon.

9. For **claims 3 and 4**, the combination of Shuholm, Cooper and Watanabe do not teach the use of transmit or receive expansion ports. Lydon teaches the expansion port limitation absent from the teachings of Shuholm, Cooper and Watanabe by disclosing the use of multiple expansion conductors (ports) in a matrix switch core with a large number of inputs and outputs **[col. 4 lines 45-48 and figure 3]** (claim 3: wherein said at least one router component further comprises a transmit expansion port; claim 4: wherein said at least one router component further comprises at least one receive expansion port). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use input and output expansion ports in Shuholm's invention to avoid collisions at the switch core.

10. **Claims 5 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lydon in view of Shuholm and Watanabe.

11. For **claim 5**, Lydon teaches a routing switch made up of four 256x256 routers **[col. 4 line 49]** (a router matrix having an input side and an output side). More generically, the router matrix is made up of N signal input terminals and M signal output terminals **[col. 3 lines 20-25]** (N data inputs coupled to the input side, M data outputs coupled to the output side).

12. Lydon does not teach the use of first and second reference inputs. Shuholm teaches the first and second reference inputs absent from the teachings of Lydon by disclosing a router receiver with an input for the first two channels of an AES signal **12** (first reference input) and a

second input for the third and fourth channels of an AES signal **13** (second reference input) **[figure 4]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a first reference input and a second reference input in Lydon's invention to allow for "channel swapping" **[Shuholm, col. 1 line 33]**.

13. The combination of Lydon and Shuholm disclose the use of clock signals (reference signals) **[Shuholm, col.2 lines 30-35]** and "channel swapping" according to a user's request **[Shuholm, col. 1 lines 30-35]**. The combination of Lydon and Shuholm does not teach the selective application of a clocking signal. Watanabe teaches an integrated circuit that uses a two mode selector that selects either a second clocking signal or allows a first clocking signal to be applied redundantly **[0028, figure 1]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Watanabe's selection circuit in Lydon's invention to allow for different sources to be used as a clocking signal **[Watanabe, 0008-0009]**.

14. For **claim 13**, the combination of Lydon, Shuholm and Watanabe disclose a hardware structure that operates on independent or redundant clock signals (reference signals) **[Watanabe, figure 1]**. Additionally, Watanabe's selector allows the router to operate without having to make modifications at the hardware level.

15. **Claims 6 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lydon in view of Shuholm and Watanabe as applied to **claim 5** above, and further in view of Donak et al. (US Pat 6,330,316), hereinafter referred to as Donak.

16. For **claim 6**, the combination of Lydon and Shuholm do not teach the use of a routing engine. Donak teaches the routing engine limitation absent from the teachings of Lydon and

Shuholm by disclosing a routing engine **120** interfaces with a switching matrix **100** and terminal trunk lines **150 [figure 1]** (wherein said broadcast router further comprises a routing engine).

17. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a routing engine in Lydon's invention to determine the proper output interface to route information to a destination.

18. For **claim 7**, Lydon does not teach the use of a reference select circuit. Shuholm teaches the reference select circuit limitation absent from the teachings of Lydon by disclosing a pair of selector circuits **20,22** (wherein said broadcast router further comprises a reference select circuit) is used to assign data from the channel buffers to an output stream or to the position in an output stream **[col. 2 lines 40-43 and figure 4]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a reference select circuit in Lydon's to perform "channel swapping".

19. **Claims 8 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuholm in view of Watanabe.

20. For **claim 8**, Shuholm teaches a digital audio receiver with multi-channel swapping **[title]**, used in a broadcast router **[col. 1 lines 25-35]**. The receiver has a first input for the first two channels of an Audio Engineering Society (AES) signal **12** and a second input for the third and fourth channels of an AES signal **13**(providing a broadcast router having first and second reference inputs; applying a first reference signal to said first reference input). Shuholm teaches input streams may be read in any combination depending upon a user's input to a pair of selectors **[col. 2 lines 45-50]** (if said user desires that said broadcast router operate with multiple reference signals, applying a second reference signal to said second reference input).

21. Shuholm teaches the input signals could come from multiple sources **[figure 3]**. Shuholm does not teach the use of redundant reference signals. Watanabe teaches an integrated circuit that uses a two mode selector that selects either a second clocking signal or allows a first clocking signal to be applied redundantly **[0028, figure 1]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Watanabe's selection circuit in Shuholm's invention to allow for different sources to be used as a clocking signal **[Watanabe, 0008-0009]**.

22. For **claim 15**, the combination of Shuholm and Watanabe disclose a hardware structure that operates on independent or redundant clock signals (reference signals) **[Watanabe, figure 1]**. Additionally, Watanabe's selector allows the router to operate without having to make modifications at the hardware level.

23. **Claims 9 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuholm and Watanabe as applied to **claim 8** above, and further in view of Cooper.

24. For **claims 9 and 10**, which depend from **claims 8 and 9 respectively**, Shuholm teaches a pair of reference select circuits **20,22** (claim 9: providing a reference select circuit) interface with a matrix in a router **[col. 2 line 56 and figure 4]** (claim 9: reference-signal demanding components; claim 10: wherein said reference signal components are reference-signal insensitive).

25. Shuholm does not teach the selector circuits determine whether or not errors were found in the reference signals. Cooper teaches a selection circuit that passes an input signal as a reference signal when the reference signal has encountered an error, namely the reference signal is missing **[col. 16 lines 25-28]**. It would have been obvious to a person of ordinary skill in the

art at the time of the invention to use Cooper's selection circuit in Shuholm's invention to provide an adjustable way to synchronize signals by allowing a clocking signal to come from more than one source **[Cooper, col. 4 lines 30-40]**.

26. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shuholm in view of Cooper and Watanabe as applied to **claim 1** above, and further in view of Bytheway ("Is Your Plant Infrastructure Up to Handling Multichannel Digital Audio").

27. For **claim 12**, Shuholm discloses transmission of information according to an AES standard **[figure 4]**. The combination of Shuholm, Cooper and Watanabe does not disclose a the alignment of more than one signal to a reference signal. Bytheway discloses a situation where two different signals, arriving at different times, are aligned to the same reference window **[page 4, 1st paragraph of the 2nd column]**. Bytheway's invention locks (a non-continual manner) audio sources to a common reference input **[page 2 1st paragraph of Synchronization and Phasing]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to align two different signals to a reference signal in Shuholm's invention to conform to an AES standard **[Bytheway, page 3 AES- 1997 – Quick Summary]**.

28. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lydon in view of Shuholm and Watanabe as applied to **claim 5** above, and further in view of Bytheway.

29. For **claim 14**, the combination of Lydon, Shuholm and Watanabe disclose the use of information transmitted according to an AES standard **[Shuholm, figure 4]**. The combination of Lydon, Shuholm and Watanabe does not disclose the alignment of more than one signal to a reference signal. Bytheway discloses a situation where two different signals, arriving at different times, are aligned to the same reference window **[page 4, 1st paragraph of the 2nd column]**.

Bytheway's invention locks (a non-continual manner) audio sources to a common reference input **[page 2 1st paragraph of Synchronization and Phasing]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to align two different signals to a reference signal in Lydon's invention to conform to an AES standard **[Bytheway, page 3 AES-1997 – Quick Summary]**.

30. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shuholm in view of Watanabe as applied to **claim 8** above, and further in view of Bytheway.

31. For **claim 16**, the combination of Shuholm and Watanabe disclose the use of information transmitted according to an AES standard **[Shuholm, figure 4]**. The combination of Shuholm and Watanabe does not disclose the alignment of more than one signal to a reference signal. Bytheway discloses a situation where two different signals, arriving at different times, are aligned to the same reference window **[page 4, 1st paragraph of the 2nd column]**. Bytheway's invention locks (a non-continual manner) audio sources to a common reference input **[page 2 1st paragraph of Synchronization and Phasing]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to align two different signals to a reference signal in Shuholm's invention to conform to an AES standard **[Bytheway, page 3 AES- 1997 – Quick Summary]**.

Response to Arguments

32. Drawing Confirmation Request

33. The Examiner has reviewed the current application file and it appears there is no figure 3. The PCT publication also appears to be missing figure 3.

34. Argument:

35. The two AES source inputs of Shuholm are not reference inputs and Shuholm has not cotemplated two reference inputs.

36. Response:

37. The Examiner agrees with the applicant with regards to the fact that well-known reference inputs are used for timing purposes and synchronization **[page 7 of Applicant's response]**. Shuholm uses the AES information for the same purpose as the reference input by using the AES information to extract clocking (timing) information **[Shuholm, col. 2 lines 30-35]**. Given that Shuholm extracts clocking information from each signal figure 4 shows that Shuholm contemplated two reference inputs by showing separate inputs for the left and right channels.

38. Argument:

39. While Shuholm employs clock data to write and output audio streams from the FIFO modules, nowhere does Shuholm disclose or suggest switching clock data extracted from the digital audio streams received at the decoders.

40. Response:

41. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In this case, the combination of Shuholm and Cooper disclose the feature of switching clock signals. For example, figure 22 of Cooper discloses an Integrated Circuit U435 that is used to switch clocking signals. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

42. Argument:

43. By combining the teachings of Cooper with those of Shuholm, the result would at most by one of the AES input streams of Shuholm being used as reference signal in the event a reference signal in Cooper is missing. Even in such a substitution, there is still only one reference signal. In contrast, we use an input reference signal as two reference signals.

44. Response:

45. Each decoder of Shuholm extracts clocking information from each received AES channel, which suggests there is more than one reference input **[Shuholm, col. 2 lines 30-35, figure 4]**. The combination of Shuholm and Cooper disclose the concept of using a single reference signal as two reference signals because Cooper discloses that when one clocking signal is received is missing (error), a clocking signal, from a different source, is selected **[Cooper, col. 16 lines 25-28]**.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY M. RUTKOWSKI whose telephone number is (571)270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey M Rutkowski
Patent Examiner
10/07/2008

/Hassan Kizou/
Supervisory Patent Examiner, Art Unit 2419